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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/648,886

08/26/2003

Monte Manning

MI22-2374

4873

21567

7590

11/22/2005

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EXAMINER

NADAV, ORI

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/648,886	Applicant(s) MANNING, MONTE	
	Examiner Ori Nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 40-58 and 70 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 40-58 and 70 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/09/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: The disclosure does not include the section "summary of the invention".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 40-47, 56-58 and 70 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification recites first and second conductive lines being electrically isolated from one another laterally by intervening insulating spacers. There is no support for the claimed limitations of first conductive lines being electrically isolated from the second conductive lines, as recited in claim 40.

There is no support for the claimed limitations of individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected

with the electrically insulating oxide material over the respective individual first series conductive lines, as recited in claim 56.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 48-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toru (Jp 06-097300) in view of Lur et al. (5,413,962).

Regarding claim 48, Toru teaches in figure 1 and related text

a layer of electrically insulating material 3;

a series of alternating first and second conductive lines 1, 11 directly over the layer of insulating material, the first and second conductive lines having respective lateral widths and being spaced and positioned laterally adjacent one another; and

intervening strips of insulating material 4 having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines, the first conductive lines and the second conductive lines being separated from one another laterally solely by the intervening strings of insulating material, the first conductive lines being electrically isolated from the second conductive lines laterally by the intervening strips of insulating material, and none of the first and

second conductive lines overlapping any immediately laterally adjacent first or second conductive lines.

Toru does not explicitly state that the device is formed on a semiconductive substrate.

Lur et al. teach in figure 11 forming the device on a semiconductive substrate 20.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Toru's device on a semiconductive substrate in order to provide support for the device.

Regarding claim 49, Toru does not teach first conductive lines are disposed directly on the electrically insulating layer. Lur et al. teach in figure 11 and related text first conductive lines 40 are disposed directly on the electrically insulating layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the first conductive lines in Toru's device directly on the electrically insulating layer in order to simplify the processing steps of making the device.

Regarding claim 50, Toru teaches in figure 1 and related text first conductive lines have a substantially common lateral cross sectional shape and second conductive lines have a substantially common lateral cross sectional shape, wherein the first conductive lines' lateral cross sectional shape being different from the second conductive lines' lateral cross sectional shape.

Regarding claim 51, Toru does not teach first and second conductive lines constitute the same material. Lur et al. teach in figure 11 and related text teach first and second conductive lines 40 constitute the same material. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the first and second conductive lines of the same material in Toru's device in order to simplify the processing steps of making the device.

Regarding claims 52 and 54, Toru teaches in figure 1 and related text first 11 and second 1 conductive lines constitute different materials, wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

Regarding claim 53, Toru does teach first conductive lines predominately comprise undoped polysilicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first conductive lines predominately comprise undoped polysilicon in Toru's device in order to adjust the conductivity of the lines according to the application at hand.

Claims 40-41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoltz et al. (5,407,860) in view of Lur et al.

Regarding claim 40, Stoltz et al. teach in figure 5 and related text an Integrated circuitry comprising:

an electrically insulating layer 50;

a series of alternating first and second conductive lines 51-53 spaced and positioned laterally adjacent one another directly over the insulating layer 30, the first lines and the second lines having respective line tops, and

intervening insulating spacers 56 laterally between the first and second conductive lines, the spacers having respective spacer tops that are substantially coplanar with one or more of the first and/or second line tops, the first conductive lines being electrically laterally isolated from the second conductive lines, and the series of first or second conductive lines can provide cross talk shielding for the other series.

Stoltz et al. do not explicitly state that the device is formed on a semiconductive substrate, and that the first conductive lines are electrically isolated from the second conductive lines such that the series of first or second conductive lines provide cross talk shielding for the other series.

Lur et al. teach in figure 11 forming the device on a semiconductive substrate 20.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Stoltz et al.'s device on a semiconductive substrate and to electrically isolate the first conductive lines from the second conductive lines such that the series of first or second conductive lines provide cross talk shielding for the other series in order to provide support for the device, and in order to use the device in an application which requires cross talk shielding, respectively.

Regarding claim 41, Stoltz et al. teach in figure 5 and related text at least some of the individual laterally adjacent first and second series lines are disposed directly on the electrically insulating layer.

Regarding claim 43, Stoltz et al. teach in figure 5 and related text the first and second conductive lines constitute the same materials.

Claims 42, 44-47 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoltz et al. (5,407,860) and Lur et al., as applied to claim 40 above, and further in view of Toru.

Regarding claim 42, Stoltz et al. and Lur et al. teach substantially the entire claimed structure, as recited in claim 42, including first conductive lines have a substantially common lateral cross sectional shape and second conductive lines have a substantially common lateral cross sectional shape. Stoltz et al. and Lur et al. do not teach first conductive lines' lateral cross sectional shape being different from the second conductive lines' lateral cross sectional shape.

Toru teaches in figure 1 first conductive lines' lateral cross sectional shape being different from the second conductive lines' lateral cross sectional shape.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape in Stoltz et al. and Lur et al.'s device in order to improve the cross-talk shielding of the device.

Regarding claims 44 and 46, Stoltz et al. and Lur et al. do not teach first and second conductive lines constitute different materials, wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal. Toru teaches in figure 1 and related text first 11 and second 1 conductive lines constitute different materials, wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first and second conductive lines constitute different materials, wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal in Stoltz et al. and Lur et al.'s device in order to adjust the conductivity of the lines according to the application at hand.

Regarding claim 45, Stoltz et al. and Lur et al. do teach first conductive lines predominately comprise undoped polysilicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first conductive lines predominately comprise undoped polysilicon in Stoltz et al. and Lur et al.'s device in order to adjust the conductivity of the lines according to the application at hand.

Regarding claim 47, Stoltz et al. and Lur et al. do teach a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate. Toru teaches in figure 1 and related text a plurality of the series of the first and second

conductive lines at multiple elevations relative to the substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate in Stoltz et al. and Lur et al.'s device in order to improve the cross-talk shielding of the device.

Regarding claim 70, Stoltz et al. and Lur et al. do teach first conductive lines and the second conductive lines are electrically isolated from one another laterally solely by the spacers. Toru teaches in figure 1 and related text first conductive lines and the second conductive lines are electrically isolated from one another laterally solely by the spacers. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first conductive lines and the second conductive lines are electrically isolated from one another laterally solely by the spacers in Stoltz et al. and Lur et al.'s device in order to reduce the size of the device.

Claims 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toru in view of Miyanaga et al. (5,418,187).

Regarding claim 56, Toru teaches in figure 1 and related text an Integrated circuitry comprising:

an electrically insulating layer 3;

a series of first conductive polysilicon lines 11 over the electrically insulating layer, the first series conductive lines having individual pairs of respective sidewalls;

electrically insulative oxide material 4 on and in contact with respective first series conductive lines, a top of the oxide material over at least some of the first series conductive lines, defining a first plane;

a plurality of insulative oxide sidewall spacer pairs 4, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulating oxide material over the respective individual first series conductive lines;

individual first series conductive lines being effectively insulated by the electrically insulating layer 3, the respective sidewall spacer pairs 4, and the respective insulating oxide material 4; and

a series of second conductive aluminum-containing lines 1 having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being over the electrically insulating layer.

Regarding the claimed limitations of a second plane that is coplanar with said first plane, since the edge of the second conductive aluminum-containing line 11 is in contact with the edge of the top part of the electrically insulative oxide material 4, then at least at that point, the planes of both materials are coplanar.

Toru does not teach an electrically insulative layer being borophosphosilicate glass (BPSG) layer over a semiconductive substrate.

Miyanaga et al. teach in figure 1E and related text an electrically insulative borophosphosilicate glass (BPSG) layer 11 over a semiconductive substrate 100. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an electrically insulative borophosphosilicate glass (BPSG) layer over a semiconductive substrate in Toru's device in order to promote surface tension, to obtain higher yield and reliability, and to provide support to the device, respectively. The combination is motivated by the teachings of Miyanaga et al. who point out the advantages of using an electrically insulative borophosphosilicate glass (BPSG) layer over a semiconductive substrate (column 2, lines 13-68, and column 9, lines 5-12).

Regarding claim 57, Toru does not teach first series conductive lines having elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first series conductive lines having elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms in Toru's device, in order to provide better protection for the device without increasing the size of the device.

Regarding claim 58, Toru teaches in figure 1 and related text individual second series lines have substantially a common lateral cross sectional shape.

Response to Arguments

Applicant argues that there is support for the claimed limitations of first conductive lines being electrically isolated from the second conductive lines, as recited in claim 40, because the first conductive lines are used as cross talk shielding, and if the cross-talk shielding is electrically connected to the interconnect lines, as implied in the office action, then capacitive coupling in the cross-talk shielding may upset the circuits containing the interconnect lines, and such an electrical connection may frustrate the providing of cross-talk shielding.

Claim 40 recites one integrated circuit comprising first conductive lines and second conductive lines, wherein the first conductive lines are used as cross talk shielding, because of capacitive coupling between the elements of the first conductive lines. Since the first conductive lines and the second conductive lines are used the same circuit, and applicant did not provide any special arrangement for both conductive lines to be connected to two separate circuits and/or power supplies, then there must be electrical connection there-between. Furthermore, the first conductive lines are used as cross talk shielding, in order to prevent capacitive coupling between the elements of the first conductive lines. Certainly, since there is capacitive coupling between the elements of the first conductive lines, there will be capacitive coupling between the first conductive lines and the second conductive lines (since now the second conductive lines is located adjacent to the elements of the first conductive lines). This capacitance coupling means that there is no electrical isolation between the first conductive lines and the second conductive lines.

Applicant argues that there is support for the claimed limitations of first conductive lines being electrically isolated from the second conductive lines, as recited in claim 40, because an artisan would recognize that the conductive lines providing the cross-talk shielding might be grounded, and thus require electrical isolation of the cable conductor from the cable shielding.

There is no support in the specification, as filed, for electrical isolation of the cable conductor from the cable shielding. Furthermore, the disclosure states that the conductive lines providing the cross-talk shielding do not have to be grounded.

Applicant argues that there is support for the claimed limitations of electrically insulative oxide material on and in contact with respective first series conductive lines over the respective individual first series conductive lines, as recited in claim 56, because figure 6 and related text provide support thereof.

Applicant states that claim 56 reads on the embodiment of figure 6. Figure 6 depicts electrically insulative oxide material 18 on and in contact with respective first series conductive lines 16 and adjacent to the respective individual first series conductive lines 16. There is no support for the claimed limitations of electrically insulative oxide material 18 on and in contact with respective first series conductive lines 16 over the respective individual first series conductive lines 16, as recited in claim 56.

The rest of Applicant's arguments with respect to claims 40-58 and 70 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660.

The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Ori Nadav', is positioned above the printed name.

O.N.
11/19/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800